Claim Rejections - 35 U.S.C. §102

Claims 50-54 and 56, prior to amendment, were rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki (U.S. Patent No. 4,471,525).

Base claim 50 has been amended to recite:

> "...forming a single layer dielectric lining on the surface of said trench; forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;"

language, which further distinguishes the presently claimed invention from Sasaki.

Sasaki discloses forming multiple dielectric layers 116 and 117 (figure 8b of Sasaki) into a trench, which are covered with polycrystalline silicon layer 118. These three layers are etched and form spacers 120 residing over both dielectric layers 116 and 117 (figure 8c of Sasaki).

However, Sasaki clearly does not teach or suggest forming a single layer dielectric lining on the surface of said trench over and in direct contact with said single layer dielectric lining, a feature of the presently claimed invention as relied for amendment.

Thus, claim 50, as presently amended, is patentable over the art of record and thus place dependent claims 51-54 and 56 as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 50-54 and 56, under 35 U.S.C. §102(b), as being anticipated by Sasaki, is overcome.

Claim Rejections - 35 U.S.C. §103

Claims 25-31, 33-38, 40-41 and 43, prior to amendment, were rejected under 35 U.S.C. §103(a) as being as being unpatentable over Sasaki in view of Kameyama (U.S. Patent No. 4,472,240).

Base claims 25 and 34 have been amended to recite:

> "...forming a single layer dielectric lining on the surface of said first trench; forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;"

language, which further distinguishes the presently claimed invention from Sasaki in view of Kameyama.

Sasaki discloses forming multiple dielectric layers 116 and 117 (figure 8b of Sasaki) into a trench, which are covered with polycrystalline silicon layer 118. These three layers are etched and form spacers 120 residing over both dielectric layers 116 and 117 (figure 8c of Sasaki).

Kameyama discloses forming an isolation region with a second trench (107) into the semiconductor layer (101), using mask patterns 106a and 106b as mask patterns.

Absent the teachings of the present invention, the motivation to combine Sasaki and Kameyama is clearly lacking. Absent the teachings of the present invention, there appears to be sufficient motivation for one skilled in the art to combine the teachings of Sasaki and Kameyama to form a second trench (107 of Kameyama (figure 4e) through a conductive p+ region (119) of Sasaki (figure 8b), without having learned the benefits taught in the present invention?

Clearly, the Examiner's combination Sasaki, in view of Kameyama, lacks motivation for one skilled in the art to combine and is therefore, unfounded.

Furthermore, Sasaki, in view of Kameyama, does not teach or suggest forming a single layer dielectric lining on the surface of said first trench, or forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining, features of the presently claimed invention as relied for amendment.

Base claim 40 has been amended to recite:

> "...forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;
>
> forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;
>
> forming an oxide filler substantially devoid of other constituents in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;"

language, which further distinguishes the presently claimed invention from Sasaki in view of Kameyama.

Sasaki discloses forming multiple dielectric layers 116 and 117 (figure 8b of Sasaki) into a trench, which are covered with polycrystalline silicon layer 118. These three layers are etched and form spacers 120 residing over both dielectric layers 116 and 117 (figure 8c of Sasaki).

Kameyama discloses forming an isolation region with a second trench (107) into the semiconductor layer (101), using mask patterns 106a and 106b as mask patterns.

Absent the teachings of the present invention, the motivation to combine Sasaki and Kameyama is clearly lacking. Absent the teachings of the present invention, there appears to be

sufficient motivation for one skilled in the art to combine the teachings of Sasaki and Kameyama to form a second trench (107 of Kameyama (figure 4e) through a conductive p+ region (119) of Sasaki (figure 8b), without having learned the benefits taught in the present invention?

Clearly, the Examiner's combination Sasaki, in view of Kameyama, lacks motivation for one skilled in the art to combine and is therefore, unfounded.

Furthermore, Sasaki, in view of Kameyama, does not teach or suggest forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining, or forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide, or forming an oxide filler substantially devoid of other constituents in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler, features of the presently claimed invention as relied for amendment.

Thus, base claims 25, 34 and 40, as presently amended, are patentable over the art of record and thus place respective dependent claims 26-31, 33, 35-38, 41 and 43 and as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 25-31, 33-38, 40-41 and 43, under 35 U.S.C. §103(a) as being as being unpatentable over Sasaki in view of Kameyama (U.S. Patent No. 4,472,240), is overcome.

Additional Information

Attached hereto (**Appendix A**) is a marked-up version of the changes made to the claims per Applicant's present response (paper 10).

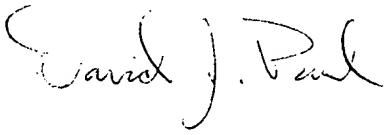
Also, attached hereto (**Appendix B**) is a clean copy of the current pending 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response (paper 10).

CONCLUSION

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,



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APPENDIX A

Following is a marked-up version of the changes made per Applicant's present response in paper 10.

In the Claims:

Claims 25, 30, 31, 34, 37, 38, 40, 50, 53 and 54 have been amended as indicated below.

25. (Twice Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said substrate assembly at the bottom of said first trench by using said [semiconductive] spacer as an etching guide;

forming [an] a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said substantially uniform insulative material.

30. (Amended) The process as recited in claim 25, wherein said step of forming [an] said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. (Amended) The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same type material.

34. (Twice Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;
forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming [an] a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said substantially uniform insulative material;

planarizing said substantially uniform insulative material;

wherein said process uses only one mask to form said device isolation.

37. (Amended) The process as recited in claim 34, wherein said step of forming [an] said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. (Amended) The process as recited in claim 34, wherein said substantially uniform insulative material and said single layer dielectric lining are the same type material.

40. (Twice Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler substantially devoid of other constituents in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

50. (Twice Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming [an] substantially uniform insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said substantially uniform insulative material.

53. (Amended) The process as recited in claim 50, wherein said step of forming [an] a substantially uniform insulative material comprises:
annealing said semiconductor assembly in the presence of an oxidizing agent.

54. (Amended) The process as recited in claim 50, wherein said substantially uniform insulative material and said dielectric lining are the same type material.

56. The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.

APPENDIX B

Following is a copy of the current pending claims 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response in paper 10.

25. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said substrate assembly at the bottom of said first trench by using said spacer as an etching guide;

forming a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said substantially uniform insulative material.

26. The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

27. The process as recited in claim 25, wherein said spacer is formed from an oxidizable material.

28. The process as recited in claim 25, wherein said spacer is formed of oxide.

29. The process as recited in claim 25, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

30. The process as recited in claim 25, wherein said step of forming said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same type material.

33. The process as recited in claim 25, wherein said process uses only one mask to form said device isolation.

34. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;

forming a substantially uniform insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said substantially uniform insulative material;

planarizing said substantially uniform insulative material;

wherein said process uses only one mask to form said device isolation.

35. The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

36. The process as recited in claim 34, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

37. The process as recited in claim 34, wherein said step of forming said substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. The process as recited in claim 34, wherein said substantially uniform insulative material and said single layer dielectric lining are the same type material.

APPENDIX B

40. A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler substantially devoid of other constituents in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

41. The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region.

43. The process as recited in claim 40, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

50. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming substantially uniform insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said substantially uniform insulative material.

51. The process as recited in claim 50, wherein an overall depth of said trench is two times the depth of a bordering diffusion region.

52. The process as recited in claim 50, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a trench.

53. The process as recited in claim 50, wherein said step of forming a substantially uniform insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. The process as recited in claim 50, wherein said substantially uniform insulative material and said dielectric lining are the same type material.

56. The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.